

This listing of claims will replace all prior versions and listings of claims in the application.

LISTING OF CLAIMS

1. (Currently amended) A method of fabricating a semiconductor chip for direct attachment to a carrier, said method comprising the steps of:

providing a partially manufactured chip having a top surface;

applying a metal layer over said top surface of said chip;

applying a passivation layer over said metal layer;

selectively removing a portion[[s]] of said passivation layer to ~~create one or more~~ define an opening[[s]] exposing a portion[[s]] of said metal layer; and

forming a solderable metal contact region[[s]] on said ~~one or more~~ opening[[s]],

wherein said solderable metal contact region[[s]] is suitable for electrically connecting to said carrier [[when]] upon positioning said chip ~~is positioned~~ face down on said carrier, suppl[[ied]]ying [[with]] a thin layer of solder to said solderable metal contact region, and applying heat[[ed]] to the thin layer of solder.

2. (Currently amended) The method as in claim 1 wherein said ~~one or more~~ solderable metal contact regions ~~is made of~~ comprises a material[[s]] selected from the group consisting of a TiCu metal layer combination, a TiNiAg metal layer combination and an AlNiVCu metal layer combination.

3. (Currently amended) The method as in claim 1 wherein said metal layer ~~[[is]]~~comprises aluminum.
4. (Currently amended) The method as in claim 1 wherein said ~~one or more~~ solderable metal contact region~~[[s are]]~~ has a thickness of approximately 1 μm ~~[[thick]]~~.
5. (Currently amended) A semiconductor chip suitable for being directly connect~~[[ing]]~~ed to a carrier, said semiconductor chip comprising:

a metal layer applied to a top surface of said chip;

a passivation layer applied over said metal layer defining an ~~such that portions of said~~
~~passivation layer is selectively removed to create one or more opening~~~~[[s]]~~, said opening
exposing a portion~~[[s]]~~ of said metal layer; and

~~one or more~~ a solderable metal contact region~~[[s]]~~ disposed ~~formed~~ on each of said ~~one or~~
~~more~~ opening~~[[s;]]~~,

wherein said solderable metal contact region~~[[s]]~~ is suitable for electrically connecting to
said carrier when said chip is positioned face down on said carrier, supplied with a thin
layer of solder, and heated.
6. (Currently amended) The semiconductor chip as in claim 5 wherein said ~~one or more~~
~~solderable metal contact regions is made of~~ comprises a material~~[[s]]~~ selected from the
group consisting of a TiCu metal layer combination, a TiNiAg metal layer combination,
and an AlNiVCu metal layer combination.
7. (Currently amended) The semiconductor chip as in claim 5 wherein said metal layer
~~[[is]]~~comprises aluminum.

8. (Currently amended) The semiconductor chip as in claim 5 wherein said ~~one or more~~ solderable metal contact region~~[[s are]]~~ has a thickness of approximately 1 μm ~~[[thick]]~~.
9. (Currently amended) A ~~Lateral Discrete Power~~ ~~[[S]]~~ semiconductor ~~MosFET~~ device~~[[C]]~~ comprising:
- (a) ~~— a semiconductor substrate;~~
 - (~~[[b]]~~) ~~a~~ at least one a first doped region defined in ~~[[said]]~~ a semiconductor substrate forming at least one, said first doped region comprising a source;
 - (~~[[c]]~~) ~~a~~ at least one a second doped region defined in ~~said semiconductor substrate forming at least one, said second doped region comprising a drain;~~
 - (~~[[d]]~~) ~~c~~ a first connectivity layer at least one comprising a first runner and at least one a second runner, wherein said at least one first runner ~~[[is]]~~ being ~~operatively connected to said at least one first doped region and said at least one second runner~~ ~~[[is]]~~ being ~~operatively connected to said at least one second doped region~~ ~~[[.]]~~;
 - (~~[[e]]~~) ~~d~~ a second connectivity layer operatively connected to said first connectivity layer and having at least one comprising a third runner and at least one a fourth runner, wherein said at least one third runner ~~[[is]]~~ being ~~operatively connected to said at least one first runner and said fourth runner~~ ~~[[is]]~~ being ~~operatively connected to said at least one second runner.~~
 - (~~[[f]]~~) ~~e~~ ~~[[A]]~~ a third connectivity layer having at least one comprising a first pad operatively connected to said at least one third runner and at least one a second pad operatively connected to said at least one fourth runner.
10. (Currently amended) ~~[[A]]~~ The semiconductor device of ~~as in~~ claim 9 wherein each of ~~said at least one first and second pads~~ has at least one of a first copper pillar ~~[[or]]~~ and a

~~[[one]] metal layer disposed thereon and said at least one first pad said at least one second pad arranged in a substantially checker board pattern.~~

11. (Currently amended) ~~[[A_]]~~The semiconductor device ~~[[of]]~~as in claim 10 wherein said at least one first pad is interleaved with said at least one second pad.
12. (Currently amended) ~~[[A]]~~The semiconductor device ~~[[of]]~~as in claim 9 wherein said at least one first doped region is a source is a source for a transistor and said at least one second doped region is a drain is a drain for a transistor.
13. (Currently amended) ~~[[A]]~~The semiconductor device ~~[[of]]~~as in claim 12 wherein said at least one source and at least one said drain are laid out in a substantially elongated shape, and wherein said at least one source ~~[[are]]~~is interleaved with said at least one drain.
14. (Currently amended) ~~[[A]]~~The semiconductor device ~~[[of]]~~as in claim 12 further comprising a plurality of the sources and drains.
15. (Currently amended) A ~~[[L]]~~lateral ~~[[D]]~~discrete ~~[[P]]~~power MosFETMOSFET device comprising:
 - (a) ~~semiconductor substrate;~~
 - ~~[[b]]~~a at least one a first doped region defined in ~~[[said]]~~a semiconductor substrate forming at least one a source;
 - ~~[[c]]~~b at least one a second doped region in said semiconductor substrate forming at least one a drain; and
 - ~~[[d]]~~c a first connectivity layer,

wherein a first portion of the first connectivity layer is operatively connected to said ~~first connectivity layer~~ first doped region and a second portion of the first connectivity layer is operatively connected to said ~~at least one~~ second doped region.

16. (Currently amended) ~~[[A]]The~~ ~~[[L]]lateral discrete power semiconductor~~ MOSFET device ~~[[of]]as in claim 15 wherein said further comprising a second conductivity~~ connectivity layer ~~[[is]]~~ operatively connected to said ~~at least one second~~ first doped region through said first ~~conductivity~~connectivity layer.
17. (Currently amended)~~[[A]]The~~ lateral discrete power ~~semiconductor~~ MOSFET device ~~[[of]]as in claim 16 wherein said second conductivity~~ connectivity layer is operatively connected to said ~~at least one~~ second doped region through said first ~~conductivity~~connectivity layer and using a portion of said first ~~conductivity~~connectivity layer for such connection.
18. (Currently amended) ~~[[A]]The~~ lateral discrete power ~~semiconductor~~ MOSFET device ~~[[of]]as in claim 15, further comprising having a third conductivity~~ connectivity layer with at least one comprising a first pad and at least on a second pad of such layer, wherein said ~~at least one~~ first pad is operatively connected to the first portion of said first ~~connectivity~~connectivity layer and said ~~at least one~~ second pad is operatively connected to the second portion of said ~~second~~ first connectivity layer.
19. (Currently amended) ~~[[A]]The~~ ~~[[L]]lateral discrete power semiconductor~~ MOSFET device ~~[[of]]as in claim 18 wherein said ~~at least one~~ first pad comprises~~ ~~[[has]]~~ at least one of a first copper pillar bump~~[[or]], a copper direct attach~~ ~~[[or]], and a solder bump and at least one said second pad comprises~~ ~~[[has]]~~ at least one of a second copper pillar bump~~[[or]], a copper direct attach~~ ~~[[or]], and a solder bump.~~

20. (Currently amended) ~~[[A]]The lateral discrete [[P]]power semiconductor~~MOSFET device
~~[[of]]as in claim 19, further comprising a plurality of said first pads and a plurality of said~~
~~second pads, wherein at least one said first pads and said at least one said second pads are~~
arranged in a substantially checkerboard pattern.
21. (Currently amended) ~~[[A]]The lateral discrete [[P]]power semiconductor~~ MOSFET
device~~[[of]]as in claim 19 wherein at least one said first pad is interleaved with said at~~
~~least one second pad.~~
22. (Currently amended) ~~[[A]]The lateral discrete [[P]]power Semiconductor~~ MOSFET
device ~~[[of C]] as in claim 15 wherein said at least one source and said at least one drain~~
are laid out in a substantially elongated shape and wherein said ~~at least one source~~
~~[[are]]is interleaved with said at least one drain.~~
23. (Currently amended) The lateral discrete [[P]]power Semiconductor~~MOSFET device~~ ~~[[of~~
~~C]]as in claim 15 wherein said at least one source and said at least one drain are laid out~~
in substantially checkerboard pattern.
24. (Currently amended) A ~~[[L]]lateral discrete [[P]]power MosFET~~MOSFET device
comprising:

(a) ~~semiconductor substrate~~

~~[[b]]a at least one first doped region formed in a in said semiconductor substrate,~~
said first doped region defining a forming at least one source~~[[:]];~~

~~[[c]]b at least one second doped region formed in said semiconductor substrate,~~
said second doped region defining a forming at least one drain~~[[:]];~~

(((d)))c) a first connectivity layer comprising having at least one a first runner operatively connected to said ~~at least one~~ first doped region and ~~at least one~~ a second runner operatively connected to ~~at least one second runner operatively connected to~~ said ~~at least one~~ second doped region[:]; and

(((e)))d) a second connectivity layer comprising having at least onea first pad operatively connected to said ~~at least one~~ first runner and ~~at least one~~ a second pad operatively connected to said ~~at least one~~ second runner.

25. (Currently amended) [[A]]The [[L]]lateral discrete [[P]]power ~~MosFET~~MOSFET [[of C]]as in claim 24 wherein said first pad has at least one of a copper pillar bump, [[or one]]a copper direct die attach, and [[or one]] a solder bump disposed thereon, and said at least one second pad has at [[:east]] least one of a second copper pillar bump, [[or]]a copper direct die attach[[or]], and a [[one]] solder bump disposed thereon.
26. (Currently amended) [[A]]The [[L]]lateral discrete [[P]]power ~~MosFET~~MOSFET [[of C]]as in claim 25, further comprising a plurality of the first pads and a plurality of the second pads wherein said at least one first pad and said at least one second pad are arranged in a substantially checkerboard pattern.
27. (Currently amended) [[A]]The [[L]]lateral discrete [[P]]power ~~MosFET~~MOSFET [[of C]]as in claim 25 wherein said at least one first pad is interleaved with said at least one second pad.
28. (Currently amended) [[A]]The [[L]]lateral discrete [[P]]power ~~MosFET~~MOSFET [[of C]]as in claim 24 wherein said at least one source and at least one said drain are laid out in a substantially elongated shape and wherein said at least one source are source is interleaved with said at least one drain.

29. (Currently amended) ~~[[A]]The [[L]]lateral discrete [[P]]power MesFET-MOSFET [[of C]]as in claim 24, further comprising a plurality of the sources and a plurality of the drains wherein said at least one source and at least one drain are laid out in substantially checkerboard pattern.~~
30. (Cancelled)
31. (New) The semiconductor device as in claim 9, further comprising a plurality of the first pads and a plurality of the second pads.
32. (New) The semiconductor device as in claim 31, wherein said first pads and said second pads are arranged in a substantially checkerboard pattern.
33. (New) The semiconductor device as in claim 14, wherein said sources and said drains are laid out in a substantially checkerboard pattern.
34. (New) The lateral discrete power semiconductor MOSFET as in claim 26, wherein said first pads and said second pads are arranged in a substantially checkerboard pattern.
35. (New) The lateral discrete power semiconductor MOSFET as in claim 29, wherein said first pads and said second pads are arranged in a substantially checkerboard pattern.